

CLAIMS

What is claimed is:

- 1 1. A memory system comprising:
 - 2 a memory controller;
 - 3 an interface device coupled to the memory controller via a first signal path; and
 - 4 a plurality of memory elements removably coupled to the interface device via respective
 - 5 second signal paths, each of the second signal paths having a lower data transfer
 - 6 capacity than a data transfer capacity of the first signal path.
- 1 2. The memory system of claim 1 wherein the first signal path comprises a plurality of
- 2 substantially parallel signal lines that extend from a first end at the memory controller to a
- 3 second end at the interface device.
- 1 3. The memory system of claim 2 wherein the plurality of the signal lines is disposed within a
- 2 flexible material to form a flex cable.
- 1 4. The memory system of claim 2 wherein the first signal path further comprises a plurality of
- 2 shielding elements disposed adjacent individual signal lines of the plurality of signal lines
- 3 to shield the individual signal lines from one another.
- 1 5. The memory system of claim 4 wherein each of the shielding elements is disposed in
- 2 coaxial alignment with a respective one of the individual signal lines.
- 1 6. The memory system of claim 2 wherein the plurality of signal lines comprise conductive
- 2 traces disposed on a printed circuit board.

1 15. The memory system of claim 1 wherein at least one of the memory elements comprises a
2 plurality of memory modules coupled in parallel to the respective second signal path.

1 16. The memory system of claim 1 wherein at least one of the memory elements comprises a
2 discrete semiconductor memory device.

1 17. A method of operation within a memory system, the method comprising:
2 transmitting multiplexed data from a memory controller to an interface device at a first data
3 rate;
4 demultiplexing the multiplexed data into a plurality of data subsets within the interface
5 device; and
6 transmitting the each of the data subsets from the interface device to a respective one of a
7 plurality of memory elements at a second data rate.

1 18. The method of claim 17 wherein the second data rate is lower than the first data rate.

1 19. The method of claim 17 wherein the first data rate is an integer multiple of the second data
2 rate.

1 20. The method of claim 17 further comprising receiving the multiplexed data within the
2 memory controller.

1 21. The method of claim 17 further comprising receiving a plurality of data values from a host
2 device, and wherein transmitting multiplexed data from the memory controller to the
3 interface device comprises transmitting the plurality of data values to the interface device

4 in respective time intervals.

1 22. The method of claim 17 wherein demultiplexing the multiplexed data into a plurality of
2 data subsets comprises allocating multiplexed data received in the interface device during a
3 first time interval to a first one of the data subsets and allocating multiplexed data received
4 during a second time interval to a second one of the data subsets.

1 23. An interface device for use in a memory system, the interface device comprising:
2 a first input/output (I/O) port to receive multiplexed data from a memory controller at a
3 first signaling rate;
4 demultiplexing circuitry to demultiplex the multiplexed data into a plurality of data subsets;
5 and
6 a plurality of second I/O ports to output the plurality of data subsets to respective memory
7 elements at a second signaling rate.

1 24. The interface device of claim 23 wherein the second signaling rate is slower than the first
2 signaling rate.

1 25. The interface device of claim 24 wherein the first signaling rate is an integer multiple of the
2 second signaling rate.

1 26. The interface device of claim 23 wherein the interface device is implemented in a dedicated
2 integrated circuit device.

1 27. The interface device of claim 23 wherein the demultiplexing circuitry is configured to
2 allocate multiplexed data received during a first time interval to a first one of the data

3 subsets and to allocate multiplexed data received during a second time interval to another
4 one of the data subsets.